P-23: Transparent Amorphous Oxide Thin Film Transistors Fabricated by Solution Coating Process

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Abstract
Transparent thin film transistors (TTFTs) with zinc tin oxide (ZTO) and indium zinc oxide (IZO) channel layer by a simple and low-cost solution process were demonstrated. The fabricated TTFTs exhibited reasonable transfer characteristics with mobilities of >2 cm²/V·s.

1. Introduction
Recently, transparent oxide semiconductors (TOSs) have attracted a great deal of attention as the active layer in transparent thin film transistors (TTFTs). Compared to amorphous silicon and low temperature polycrystalline silicon (LTPS) devices, TOSs have sufficient mobility to drive active matrix OLED (AMOLED), good environmental stability, low cost, and high transparency for backplanes with large aperture ratio [1]. Among TOSs, amorphous heavy metal oxides with (n−1)d10 ns0 (n≥4) electronic configuration are promising candidates for high performance TTFT channel materials. Zinc based amorphous oxides semiconductors (AOSs) such as indium gallium zinc oxide (IGZO) [2], zinc tin oxide (ZTO) [3], and indium zinc oxide (IZO) [4] have been reported for TTFT channel layer. These amorphous oxide TFTs were fabricated on various substrates, including silicon, glass and flexible polymers, and showed high mobilities up to 40 cm²/V·s. However, most AOSs have been prepared by vacuum processes such as rf magnetron sputtering and pulse laser deposition, which require expensive equipments and result in high fabrication costs.

Solution process is alternative thin film deposition method which is a simple and low-cost pathway and enables large area coating and high throughput. Moreover, direct patterning is available through ink-jet printing, imprinting, and screen printing without complex photolithography process.

We report a simple and low-cost process to fabricate the highly transparent ZTO and IZO TFTs under ambient condition, and the performances of TTFTs using ZTO and IZO active channel layer. By a solution process using zinc, tin, and indium precursors in solvent which are capable of forming uniform and continuous thin films through spin coating, TTFTs with amorphous ZTO and IZO thin film semiconductor could be obtained.

2. Results and Discussion
Metal precursor solution for fabricating ZTO and IZO thin films was prepared by dissolving zinc(II) acetate dehydrate (Zn(CH₃COO)₂·2H₂O, Aldrich), tin(II) chloride (SnCl₂, Aldrich), and indium(III) acetate (In(CH₃COO)₃, Aldrich) in 2-methoxyethanol separately. In order to make the solution stable, the precursors were chelated with acetylacetone or diethanolamine with an equivalent molar ratio. Then, precursor solutions were mixed and stirred. Heavily boron (p+) doped silicon wafer with 120nm of thermally grown silicon dioxide (SiO₂) on top of the silicon and glass substrate coated with 200 nm of sputtered indium tin oxide (ITO) layer and 100 nm of plasma enhanced chemical vapor deposited SiO₂ layer were used in bottom gate/top contact structure for the fabrication of the ZTO and IZO TFTs (Figure 1. (a)) and TTFTs (Figure 1. (b)), respectively. The SiO₂/Si wafer and the SiO₂/ITO/glass substrate were first rinsed with acetone and isopropanol, and then cleaned with oxygen plasma treatment. The resulting solution was deposited on the SiO₂/Si wafer and the SiO₂/ITO/glass substrate by the spin coating method at 5000rpm for 30s. Finally, ZTO and IZO thin films were heat-treated at 500 °C for 1 hour in ambient air. The source and drain electrodes were deposited on the ZTO and the IZO layers through a shadow mask, using the aluminum. The channel length was 120 µm and the channel width was 1000 µm. The TFT devices were analyzed with two Keithley 236 source-measure units and a HP 4145B semiconductor parameter analyzer in the dark room.

Figure 1. Schematic cross-sectional view of (a) the TFT and (b) the TTFT structure and SEM images of (c) the ZTO TFT and (d) the ZTO TTFT.

Figure 1. (c) and (d) show cross sectional SEM images of the ZTO TFT and the ZTO TTFT. These images indicate the 20 nm thickness of the ZTO layers were deposited by spin coating and heat-treatment.
Figure 2. XRD patterns obtained from (a) the ZTO and (b) the IZO thin film with heat treatment at 500 °C for 1h in air [7,8].

Figure 2 shows the XRD patterns of the ZTO and the IZO thin film annealed at 500°C. Only a broad peak at 2θ=34° and no peak in XRD patterns indicates the ZTO and the IZO thin film is amorphous.

Figure 3. UV-vis transmittance spectra and optical images (inset) of (a) the ZTO (solid line) [7,8] and the IZO (dotted line) thin films and (b) the ZTO (solid line) and the IZO (dotted line) TTFTs.

Figure 3. (a) shows the transmission spectra of the ZTO and the IZO films on quartz substrates. The films are highly transparent (>90%) in the visible range (400–700 nm). Transparency of the films is also confirmed by the optical image in the inset of Figure 3. (a). The ZTO and the IZO TTFT devices are also highly transparent (average~80%) in the visible range (Figure 3. (a)).
Figure 5. (a) Output and (b) transfer curves of the IZO TFT with $V_{DS} = 40$V [8] and (c) transfer curve of the ZTO TFT with $V_{DS} = 20$ V.

Figure 4 shows the output curve and the transfer characteristics of with a drain voltage at 40 V for the ZTO TFT. The output curve shows the ZTO TFT is n-channel transistor and has good linear/saturation property. The electrical parameters including the saturation field effect mobility and the threshold voltage were derived from a linear fitting to the plot of the square root of drain current ($I_D$) versus gate voltage ($V_G$) using the following equation of the saturation region

$$I_D = \frac{W}{2L} \mu_{FE} (V_G - V_{th})^2$$

where $W$ and $L$ are channel width and length, respectively, $\mu_{FE}$ is the field effect mobility, $C_i$ is the capacitance per unit area of SiO$_2$ gate insulator (dielectric constant~3.9), and $V_{th}$ is the threshold voltage. The ZTO TFT has a field-effect mobility of 3.7 cm$^2$/V·s and a threshold voltage of 7.6 V. Turn on voltage ($V_{on}$) [9] is equal to 4V. $V_{on}$ directly characterizes the gate voltage required to fully ‘turn off’ the transistor in a switching application. The enhancement mode (normally off) ZTO TFT can simplify the circuit design and lower the power dissipation. The ZTO TFT exhibits a good subthreshold slope (S) 0.3 V/dec, which is quite small relatively to other solution-processed ZTO TFT [5]. The small S originates from a small amount of the interface traps in the amorphous ZTO thin film. The IZO TFT also has good n-type transistor characteristics with the field effect mobility of 7.3 cm$^2$/V·s and the threshold voltages of 2.5V (Figure 5). The subthreshold slope of the IZO TFT is 1.47 V/dec., which is lower than those of other solution-processed IZO TFT [6]. Additionally, the ZTO and the IZO TFTs show the on-off current ratios higher than $10^7$ with the low off current, which is a superior property compared to those of the solution-processed amorphous oxide TFTs (~$10^5$) [5,6]. Since the ZTO and the IZO films are very thin (10~20 nm) and amorphous, the off current can be suppressed.

The ZTO and the IZO TFTs show reasonable transistor characteristics (Figure 4. (c) and Figure 5. (c)). The field effect mobility of the ZTO and the IZO TFT are 2.1 cm$^2$/V·s and 4.6 cm$^2$/V·s, and the threshold voltages are 5.4 V and -12.7V respectively. Although the mobilities are lower than not only vacuum-deposited ones but also TFTs with SiO$_2$/Si substrate [7,8], it is a sufficient to fulfill the requirements of AMOLED, thus, the solution-processed ZTO and IZO TFT can be applicable to the backplane of the AMOLED [10]. However, both TFTs show lower on-off current ratio and poorer subthreshold slope than TFTs using SiO$_2$/Si substrate [7,8]. The on-off current ratios of the ZTO and the IZO TFTs are $1 \times 10^5$ and $1.6 \times 10^6$ respectively. High off current and low on-off current ratio probably originate from gate leakage, because the gate dielectric SiO$_2$ layer deposited using PECVD has higher leakage current than thermally grown SiO$_2$ layer and atomic layer deposited layer. Additionally, un-patterned channel layers also increase off current. The subthreshold slopes of the ZTO and the IZO TFTs are 0.7 V/dec. and 12.8 V/dec. High off current and poor roughness of glass increase subthreshold slope. We prospect the high off current characteristics can be suppressed by using other gate dielectric materials and patterned TFT structure.
3. Conclusions
We fabricated the ZTO and IZO based TTFTs using a simple and low-cost solution process instead of typical vacuum deposition methods. The TTFTs showed reasonable transfer characteristics with mobilities of >2cm²/V·s. These results provide that the solution-processed ZTO and IZO TFTs are promising devices for high performance backplane and large area display.

4. References