Low Temperature Annealed Sol-Gel Aluminum Indium Oxide Thin Film Transistors

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Abstract

Thin-film transistors (TFTs) with an aluminum indium oxide (AIO) channel layer were fabricated via a simple and low-cost sol-gel process. Effects of annealing temperature and time were investigated for better TFT performance. The sol-gel AIO TFTs were annealed as low as 350 ℃. They exhibit n-type semiconductor behavior, a mobility higher than 19 $cm^2/V\cdot s$ and an on-to-off current ratio greater than 10^8.

1. Introduction

Transparent thin film transistors (TTFTs) including oxide active channel layer are of great current interest for transparent electronics such as flat panel displays, flexible displays, radio-frequency identification tags and smart windows [1, 2, 3]. In particular, not only the research field but also the industrial field have much interest in oxide TFTs after they are considered as a prominent candidate for the backplane of AMOLED and AMLCD [4].

Metal oxide semiconductors have many advantages such as transparency due to their large band gap, high uniformity for large size fabrication, environmental stability and high field-effect. Many transparent oxide semiconductors (TOSs) such as zinc oxide [5], indium-zinc oxide [6], zinc-tin oxide [7], indium-gallium-zinc oxide [2], and indium oxide [8] have been reported for transparent channel layers in TTFTs. However, TOSs are generally prepared by vacuum-deposition methods such as rf magnetron sputtering and pulsed laser deposition which require high costs.

Solution processed thin film deposition such as a sol-gel method could offer many advantages such as simplicity, high throughput, and low-cost compared to vacuum-deposition process. In addition, it enables the direct patterning (i.e. inkjet printing and roll-to-roll process) that could replace the conventional photolithographic techniques.

2. Experimental

The metal precursor solution for the AIO channel layer was prepared by dissolving 0.1 M of indium acetate [$In(C_2H_3O_2)_3$, Aldrich] and aluminum acetylacetonate [$Al(C_5H_7O_2)_3$, Aldrich] in 2-methoxyethanol [$C_3H_8O_2$, Aldrich]. Amount of Al precursor in the precursor solution was 40 % of indium precursor. In order to form a stable solution, the indium acetate precursor was chelated with 0.4 M of ethylenediamine (EDA, $NH_2CH_2CH_2NH_2$, Aldrich). The solution was stirred at room temperature for half an hour to make a transparent and homogeneous solution. After sufficient reaction, the solution was filtered through a 0.22 ㎛ syringe filter (PTFE, GE) and spin-coated at a speed of 5000rpm atop of the SiO_2/Si substrate for 30 s. The 50W of oxygen plasma treatment was applied for 5mins just before the spin-coating in order to remove unnecessary organics on the substrate using conventional plasma cleaner. A 100nm SiO_2 layer, which served as a gate dielectric, was thermally grown on the top of the heavily boron (p+) doped silicon wafer. After film deposition, it was annealed on a hot plate under air at various temperatures.

The structural and electrical properties of AIO thin films were characterized by using various analyzing tools. A thin film x-ray diffractometer (XRD, Rigaku) was used to investigate the crystallinity and crystal orientation of the film. The electrical property of AIO TFTs was analyzed by HP 4145B semiconductor parameter analyzer and probe station.

3. Results and discussion

Formation of metal oxide thin film relies heavily on annealing process in sol-gel method. In my previous work, decomposition behavior of AIO precursor solution was studied by thermogravimetric analysis (TGA, TA instrument Q50) [9]. According to the

result, annealing temperature was controlled to 300°C, 350°C, and 500°C for 1 hr. The transfer curves at a fixed V_{DS} = 40 V, displayed in figure 1, show that annealing temperature affects the electrical property of AIO TFTs clearly. As the annealing temperature increases on-current and off-current increase and transfer curves are shifted to negative voltage. The summarized electrical parameters are listed in the table 1. It is generally accepted that higher annealing temperature results in better crystallinity [10]. The better crystallinity of the film increases the carrier concentration, which is related to the shift of transfer curve, and improves electron conduction ability. The XRD patterns, shown in figure 2a, support the better crystallinity with higher annealing temperature. Clear current modulation behavior with gate bias is observed even at 300℃ annealed AIO TFT with amorphous phase. Although the mobility is low, its sub-threshold swing and on-to-off current ratio are sufficient enough to drive the electronic circuits and its low annealing temperature shows the possibility of low temperature process. It is expected that 300 ℃ annealed AIO TFT would have a chance to find new applications such as e-paper or where low temperature process is necessary [11]. In addition, its low temperature processibility allows use of various substrates such as soda-lime glass and plastic substrates.

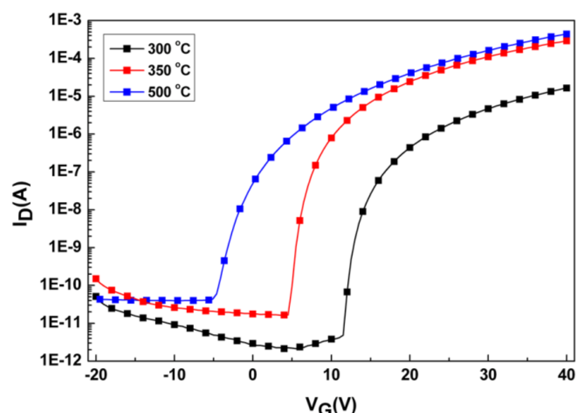
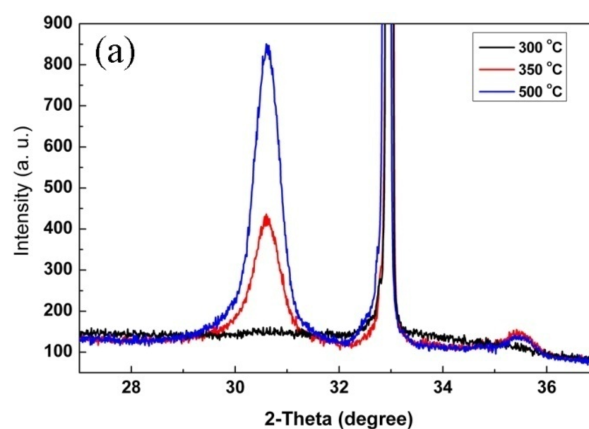


Fig. 1. Transfer characteristics for AIO TFTs with various annealing temperature for V_{DS} = 40 V with structure of L=220 ㎛ and W=1000 ㎛.

The 500℃ annealed sample shows good electron conduction property. It is generally accepted that high temperature annealing improves the crystallinity, defects level, and interface between semiconductor and gate dielectric of the films and results in better TFT performance. However, in this case, its off-current and sub-threshold swing, that are related to defects and interface, are higher than 350℃ annealed sample. The results indicate that too high temperature annealing (i.e., 500℃) deteriorates the quality of the film and generates the defects in the film and oxygen vacancy on the surface of the film by breaking the bonding between indium and oxygen or evaporation of metal cations.

TABLE 1. Electrical properties of AIO TFTs annealed at various temperature.

Temp. (℃)	μ (cm^2/V·s.)	I_{on}/I_{off}	S (V/dec)
300	0.8	7.7×10^6	0.6
350	5.7	1.8×10^7	0.5
500	11.5	1.1×10^7	1.3



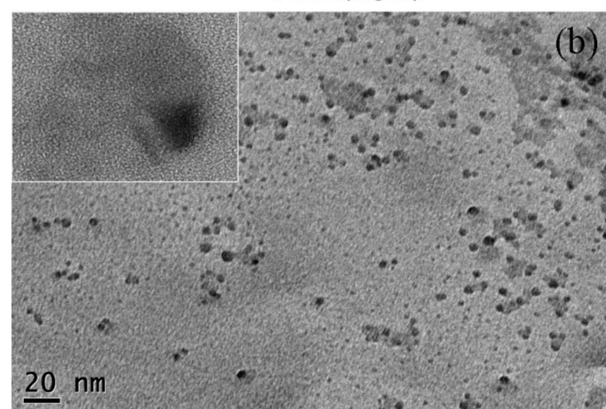


Fig. 2. (a) θ-2θ XRD analysis of AIO thin films with various annealing temperature on SiO_2/Si substrate. (b) TEM surface image of AIO thin-film annealed at 350℃ for 1h and magnified image of nano size crystal (inset).

Figure 2b shows the TEM surface image of AIO thin-film annealed at 350℃ for 1 hr. The image

indicates that the film is partially crystallized. The size of crystallites are around 3-5nm and they are distributed over the film. The inset shows the magnified image of crystallite. The back part with grid is well crystallized section while white part is in amorphous phase.

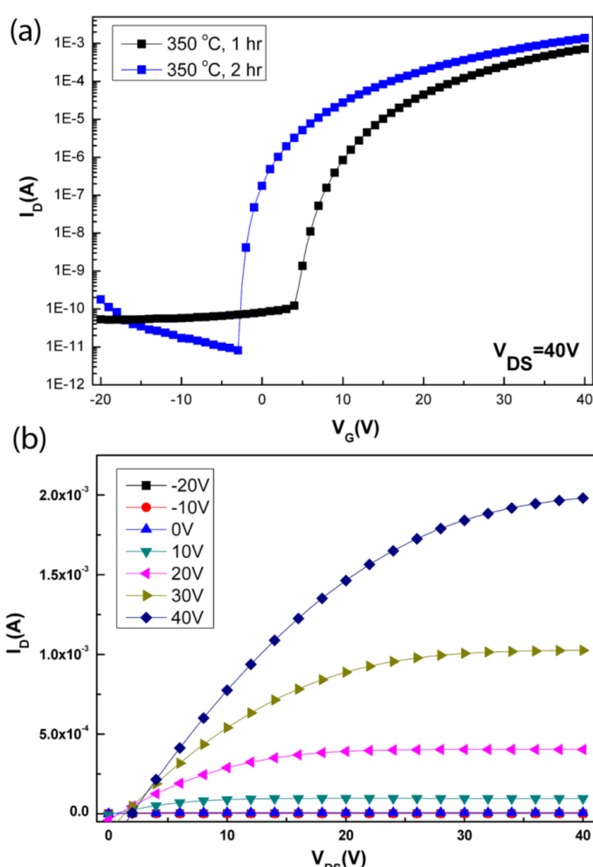


Fig. 3. (a) Transfer characteristics for AIO TFTs with various annealing time for V_{DS} = 40 V with structure of L=220 ㎛ and W=1000 ㎛. (b) Output characteristics for the AIO TFT annealed at 350℃ for 2 hrs with various gate voltages.

Effects of annealing time of the AIO TFTs were displayed in figure 3a. The effects were quite clear at the early stage of variation (i.e. 1 hr and 2 hrs). However, any change in electrical property was not observed with the annealing time over 2 hrs. As the annealing time increases, the on-current and level of defects were improved and the transfer curve was shifted to negative voltage. The result indicates that longer annealing time elevates the performance of the TFTs in terms of mobility and sub-threshold swing which are related to faster and accurate operation of the devices.

Figure 3b shows the drain current versus drain-to-source voltage (I_D-V_{DS}) output characteristics of AIO TFT, annealed at 350 ℃, for various gate voltages (V_G). Clear pinch-off and current saturation behaviors are observed in output characteristics which are essential to adopt the conventional TFT theory to explain the operation of AIO TFTs [2]. As a result, it is natural to conclude that 350 ℃ is the suitable annealing temperature for TFT application. The optimized AIO TFT exhibits channel mobility of μ = 19.6 $cm^2/V{\cdot}s$ and shows n-type semiconductor behavior with 350 ℃ annealing. The threshold voltage is around 10V, sub-threshold swing is 0.5V/decade and on-to-off ratio is 1.7×10^8 with low off-current of 8.1×10^{-12} which are compatible with the results of vacuum processed oxide TFTs.

4. Summary

We have demonstrated highly transparent aluminum indium oxide thin film transistors with simple and low-cost spin coating process. It shows good electrical properties and operates in accumulation mode on a positive gate bias. Moreover, its low annealing temperature (350 °C) promises the use of various substrates (e.g. soda-lime glass and plastic substrates). These results reveal that the solution processed AIO TFT is the suitable device for high performance display back planes and transparent electronics.

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