Low Temperature Fabrication of Aqueous Solution Processed Flexible Indium Oxide Transparent Thin-Film Transistors on a Plastic Substrate

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Abstract

An aqueous route enables the fabrication of indium oxide (IO) TFT at low temperature, below 200 ℃. The optimized IO TFT exhibits a mobility of 3.64 $cm^2V^{-1}s^{-1}$ with 200 ℃ annealing. The vacuum and humid O_2 post annealing activates the IO TFT even with 125 ℃ annealing due to the effective removal of impurities and oxidation. The flexible transparent IO TFT is fabricated on a PEN substrate and the device exhibits mobility over 4 $cm^2V^{-1}s^{-1}$ and S.S. 210 mV/dec with a turn-on voltage around 0 V. Also, the detailed stbility studied of the flexible transparent TFT will be demostrated.

1. Introduction

Metal oxide semiconductors (MOS) attract great interest for next generation display driving circuitry due to their favorable mobility, good environmental stability, and transparency.[1] The solution process allows the preparation of MOS at low cost with good large area uniformity and yields while vacuum based process, such as sputtering and ion beam assisted laser deposition, requires high cost and complex equipment[1]. Also, it enables the direct patterning, such as ink-jet printing and roll-to-roll process which could replace the conventional lithographic techniques. However, the high annealing temperature for oxide formation restricts the application of solution process.

In this study, we report a novel aqueous route for fabrication of oxide TFT at low temperature. The aqueous route allows the formation of unique structure of indium complex and low annealing temperature. The additional post annealing facilitates the formation of oxide at low temperature. Finally, the optimized IO TFT is fabricated on flexible PEN substrate which exhibits good electrical performance and bias stability.

2. Experimental

The Aqueous solutions for the IO channel layer was prepared by dissolving indium nitrate hydrate in DI water. The solution was stirred at room for 6 h to make a transparent and homogeneous solution. The aqueous solution was filtered through a 0.22 um syringe filter (PTFE, GE) and spin-coated atop of the SiO_2/Si substrate at a speed of 5krpm for 30 s. The as-deposited layer was annealed on a hot-plate under ambient atmosphere. The additional vacuum and humid O_2 post annealing was applied using rapid thermal annealing (RTA) system for 0.5 and 1 h, respectively. The optimized IO thin-film, annealed 200 ℃, is implanted on transparent TFT structure on a flexible PEN substrate. The bottom-gate, bottom-contact type structure is adopted for this device. The PEN substrate is attached on the carrier glass for the glasslike process using cool-off-type adhesive (Intelimer)[2]. The IO TFT was fabricated at low temperature, maximum process temperature of 200 ℃. After fabrication process, the flexible transparent IO TFT is easily delaminated at low temperature (below 10 ℃).

3. Results and discussion

The IO TFTs were fabricated through aqueous route with low temperature annealing. The IO TFT was activated even at 175 ℃ without any further process[3]. The Fig. 1. shows the annealing time and temperature dependency IO TFTs. As annealing temperature increases, the transfer curve tends to shift to the negative voltage due to the generation of oxygen vacancy from higher thermal energy.

The naturally born indium complex, hexa-aquo ions with centred indium cation, enables the low temperature oxide formation[4]. The optimized IO TFT, annealed at 200 ℃, exhibits mobility of 3.64 $cm^2V^{-1}s^{-1}$ and S.S. of 230 mV/dec with turn-on voltage of 0 V. Additionally, zinc cation is adopted into IO matrix to control the carrier concentration for various applications.

In order to decrease the annealing temperature the vacuum and humid O_2 post annealing were followed to the 125 ℃ ambient annealed thin-film. The vacuum annealing facilitates the condensation reaction by effectively removing the by-product water molecule and removes the

impurities which interrupt the oxide formation. In addition, the post humid O_2 annealing enables the oxidation of remaining unreacted indium species[5]. After the post annealing, the IO TFT is activated even at 125 ℃ annealing and exhibits the mobility over 3, S.S. of 0.79 with a turn-on voltage of 0 V. (Fig. 2.) This result indicates that post annealing is a proficient method to fabricates the oxide TFT at low temperature by effective removal of impurity and facilitate the oxide formation.

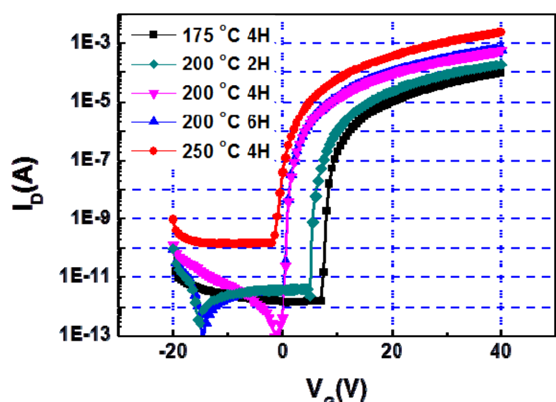

Fig. 1. Transfer characteristics of In_2O_3 TFTs according to the annealing temperature and time.

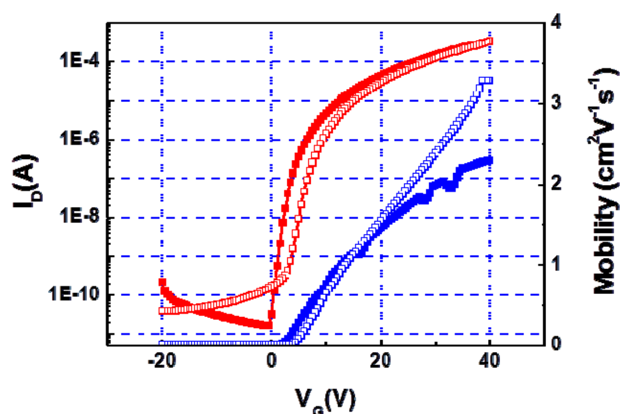

Fig.2. Transfer characteristics and mobility of the vacuum and humid O_2 post annealed In_2O_3 TFT at 125 ℃.

The transparent IO TFT is fabricated on the flexible PEN substrate. The MOSs are unique class of materials that exhibits seimconducting property and transparency, simultaneously, which are usually considered as a contradictory property. The Fig. 3. shows the photo image and electrical performance of flexible transparent TFT. The device exhibits good performance, mobility of 4.04, S.S. of 210 mV/dec, and turn-on voltage near origin. The flexible transparent TFT shows good resistance to the external positive and negative bias stress, less than 1.5 V and 0.5 V with 10000 s, respectively[3]. Additionally, the stabillity against illumination and gate bias will be demonstrated.

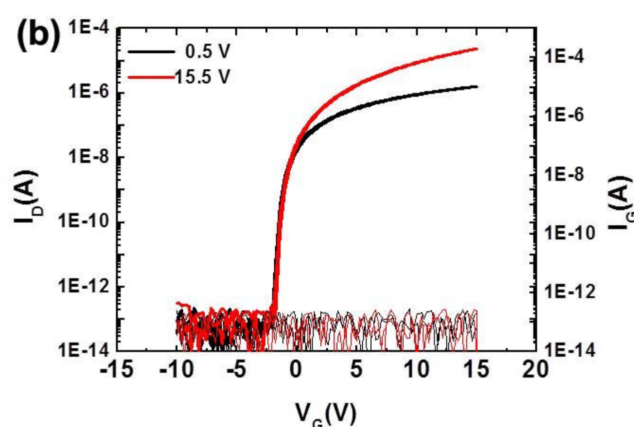

Fig. 3. Photo image (a) and transfer characteristics (b) of transparent In_2O_3 TFT on a flexible PEN substrate.

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